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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,236	03/26/2001	Masashi Asakawa	100021-00046	8733

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EXAMINER
ENCARNACION, YAMIR

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 07/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/816,236	Applicant(s) ASAKAWA ET AL.	
	Examiner Yamir Encarnacion	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. The limitation "said plurality of memory clocks" in claim 2 lacks antecedent basis. Perhaps applicant mean --said plurality of memory blocks--

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Usami* (USPN: 6,205,516 B1) in view of *Fadavi-Ardekani* (USPN: 6,401,176).

Claimed	***Usami***
1. A synchronous DRAM comprising:	See figure 1, the internal RAM 3 and the Extended RAM 4.

one memory array divided into a plurality of memory blocks;	Figure 8 shows the memory map (which reads on the claimed "memory array") divided into a plurality of blocks. Note specially, the block labeled internal RAM3 and the block labeled internal RAM4.
mode storage units so disposed in a plurality of stages as to correspond to said memory blocks, for storing control information for defining operation modes of said memory blocks;	See Figure 8, the mode register area 1 corresponding to internal RAM3 and the mode register area 2 corresponding to extended RAM4.
a setting unit for setting the control information designated by a mode setting instruction to said mode storage unit corresponding to said memory block designated by said mode setting instruction in accordance with said mode setting instruction outputted from a plurality of [controllers];	See figure 1, the memory control circuit 5a.

a mode selection unit for selecting said mode storage unit corresponding to said memory block containing a memory cell designated by an address inputted; and an access unit for executing an access operation in synchronism with a predetermined clock signal for the corresponding one of said memory blocks in accordance with the control information stored in said mode storage unit selected.	The reference meets the limitation of the claim.

Usami does not explicitly disclose that the programmable registers are programmed via instructions outputted from a plurality of controllers.

Fadavi-Ardekani discloses of multiple processors accessing a shared synchronous memory. See *Fadavi-Ardekani*, the front cover. A person of ordinary skill in the art would have found it obvious to couple multiple processors as was done by *Fadavi-Ardekani* to the synchronous memory described by *Usami* for the purpose of increasing performance. Accordingly, it would have been obvious to use multiple processors sharing the synchronous memory described by *Usami* for the purpose of increasing performance. The said processors would have read on the claimed "controllers."

As to claim 4, it would have been obvious to those of ordinary skill in the art to include the values to be placed in the registers as part of a reprogramming command. See *Usami*'s abstract.

As to claims 5 and 9, *Usami* describes the information sent on the address/data busses in column 13, lines 51-54.

As to claims 6-8, these claims do not patentably distinguish over the *Usami/Fadavi-Ardekani* combination because these claims merely recite nonfunctional descriptive material.

In the alternative as to claim 7, see figure 4, bits A0, A1, and A2.

In the alternative as to claim 8, see figure 4, bits A4, A5, and A6.

As to claim 10, values can be loaded into the registers.

As to claims 11-12, the *Usami/Fadavi-Ardekani* combination meets the limitations of the claims.

6. Claims 1 and 3-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Rao* (USPN: 6,173,356 B1) in view of *Usami*.

Claimed	***Rao***
1. A synchronous DRAM comprising:	See figure 4.
one memory array divided into a plurality of memory blocks;	See figure 4, the banks 401.

mode storage units so disposed in a plurality of stages as to correspond to said memory blocks, for storing control information for defining operation modes of said memory blocks;	See figure 4, the mode registers 415. Column 11, lines 15 - 17 states that "each memory bank 401, is associated with a corresponding mode register, and coupled thereto by the corresponding mode register bus 418."
a setting unit for setting the control information designated by a mode setting instruction to said mode storage unit corresponding to said memory block designated by said mode setting instruction in accordance with said mode setting instruction outputted from a plurality of controllers;	Column 11, lines 18-21 states that "[c]ore logic/memory controller 402 configures memory bank 401 under the control of CPUs 416a and 416b, coupled to core logic/memory controller 402 by system busses 417a and 417b, respectively."

a mode selection unit for selecting said mode storage unit corresponding to said memory block containing a memory cell designated by an address inputted; and an access unit for executing an access operation in synchronism with a predetermined clock signal for the corresponding one of said memory blocks in accordance with the control information stored in said mode storage unit selected.	It would have been obvious to those of ordinary skill in the art that *Rao* meets these limitations.

While *Rao* explicitly discloses in column 11, lines 18-19 that "Core logic/memory controller 402 configures memory bank 401 under the control of CPUs 416a and 416b," *Rao* does not explicitly disclose that the programmable registers are programmed via instructions outputted from a plurality of controllers.

Usami teaches of setting the mode registers which configure the banks 401 via a "Mode Register Set" command. See *Usami*, column 10, lines 43-52.

A person of ordinary skill in the art would have found it obvious to use the method of setting the mode registers taught by *Usami* in *Rao* given that *Rao* is silent on the exact procedure followed when setting the mode registers. Accordingly, it would have been obvious to those of

ordinary skill in the art to use a "Mode Register Set" command such as the one described by *Usami* in *Rao* because the use of the "Mode Register Set" command in *Rao* would have allowed for the mode registers to be set in accordance with the procedures followed by others in the art.

As to claim 3, the reference meets the limitation of the claim.

As to claim 4, it would have been obvious to those of ordinary skill in the art to include the values to be placed in the registers as part of a reprogramming command.

As to claims 5 and 9, see the comments made for *Rao* above.

As to claims 6-8, these claims do not patentably distinguish over the *Usami/Rao* combination because these claims merely recite nonfunctional descriptive material.

In the alternative as to claim 7, see *Rao*, figure 8, bits 0-2.

In the alternative as to claim 8, see *Rao*, figure 8, bits 4-6.

As to claim 10, values can be loaded into the registers.

As to claims 11-12, the *Usami/Rao* combination meets the limitations of the claims.

7. Claims 1, 3-10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Farrer* (USPN: 5,307,320) in view of *Fadavi-Ardekani* (USPN: 6,401,176).

Claimed	***Farrer***
1. A [synchronous] DRAM comprising:	See figure 1, the main memory 103.
one memory array divided into a plurality of memory blocks;	Figure 2a shows a card with bank0 and bank1.

mode storage units so disposed in a plurality of stages as to correspond to said memory blocks, for storing control information for defining operation modes of said memory blocks;	Figure 3 shows five programmable bank configuration registers. Column 6, lines 1-2 states that "[e]ach register is associated with a bank in the memory." See also column 13, lines 9-15.

a setting unit for setting the control information designated by a mode setting instruction to said mode storage unit corresponding to said memory block designated by said mode setting instruction in accordance with said mode setting instruction outputted from [a plurality of controllers];	Column 5, lines 54-66 states that "[t]he bank configuration registers are programmable. The registers are programmable in that software can be used to load the registers with the proper values to configure the interface to the memory bank. The register could be loaded using a menu driven software which permits the user to indicate the type of DRAM in the bank location and any other parameters required to permit access to that DRAM bank. Self-configuration software can also be used to program the registers. The self-configuration software scans the memory cards of each bank and determines the type of memory card and configuration required so that access may be gained." See also column 14, lines 24-30.

a mode selection unit for selecting said mode storage unit corresponding to said memory block containing a memory cell designated by an address inputted; and	See column 10, lines 1-31. Note that the "address remapping block translates bits 16-25 of the bank configuration register to determine the proper addressing modes of the DRAM." See also column 12, lines 27-42.
an access unit for executing an access operation in synchronism with a predetermined clock signal for the corresponding one of said memory blocks in accordance with the control information stored in said mode storage unit selected.	See column 12, lines 27-42.

Farrer does not explicitly disclose that the memory described therein is a synchronous DRAM or that the programmable registers are programmed via instructions outputted from a plurality of controllers.

Fadavi-Ardekani discloses that SDRAM technology combines DRAMs with a high-speed interface. See *Fadavi-Ardekani*, column 1, lines 27-30. *Fadavi-Ardekani* further discloses that because SDRAMs are programable, systems using SDRAM can improve bus utilization because the processor can be synchronized to the SDRAM output. See *Fadavi-Ardekani*, column 1, lines 47-50. A person of ordinary skill in the art would have found it desirable to improve bus

utilization in the environment described by *Farrer*. In light of *Fadavi-Ardekani*, a person of ordinary skill in the art would have found it obvious to modify *Farrer* so as to combine the DRAM described therein with a high-speed interface like the one described by *Fadavi-Ardekani* to achieve an SDRAM for the purpose of achieving improved bus utilization. Accordingly, it would have been obvious to those of ordinary skill in the art to combine the DRAM described by *Farrer* with a high speed interface like the one described by *Fadavi-Ardekani* because the *Farrer/Fadavi-Ardekani* combination would have achieved improved bus utilization.

Also, *Fadavi-Ardekani* discloses of multiple processors accessing a shared synchronous memory. See *Fadavi-Ardekani*, the front cover. A person of ordinary skill in the art would have found it obvious to couple multiple processors as was done by *Fadavi-Ardekani* to the synchronous memory rendered obvious by the *Farrer/Fadavi-Ardekani* combination described above for the purpose of increasing performance. Accordingly, it would have been obvious to use multiple processors sharing the synchronous memory rendered obvious by the *Farrer/Fadavi-Ardekani* combination described above for the purpose of increasing performance. The said processors would have read on the claimed "controllers."

As to claim 3, the banks described by *Farrer* read on the claimed banks.

As to claim 4, it would have been obvious to those of ordinary skill in the art to include the values to be placed in the registers as part of a reprogramming command.

As to claims 5 and 9, the portion of *Farrer* reading "[t]he register could be loaded using a menu driven software which permits the user to indicate the type of DRAM in the bank location

and any other parameters required to permit access to that DRAM bank" implies that the values are sent to the registers via a bus.

As to claims 6-8, these claims do not patentably distinguish over the *Farrer/Fadavi-Ardekani* combination because these claims merely recite nonfunctional descriptive material.

In the alternative as to claim 8, notice that in column 6, lines 50-51, *Farrer* discloses that the CAS timing filed consists of bits 8-10.

As to claim 10, values can be loaded into the registers.

As to claim 12, the reference meets the limitations of the claim.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Bolyn, P., inventor; Unisys Corp., assignee. Memory Control Unit Using a Programmable Shift Register for Generating Timed Control Signals. US patent 6,092,165. 2000 Jul 18.

Bolyn teaches of a memory with a plurality of mode registers.

Any inquiry concerning this or an earlier communication from the Examiner should be directed to Yamir Encarnacion by phone at (703) 308-5466.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

Any formal response to this action intended for entry should be mailed to Commissioner of Patents and Trademarks, Washington, D.C. 20231 or faxed to (703) 746-7239 and labeled

"FORMAL" or "OFFICIAL." Any informal or draft communication should be faxed to (703) 746-7240 and labeled "INFORMAL" or "UNOFFICIAL" or "DRAFT" or "PROPOSED" and followed by a phone call to the Examiner at the above number. Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

YEE

Yamir Encarnacion

Patent Examiner

June 23, 2002

DO HYUN YOO
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TECHNOLOGY CENTER 2100